UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/294,617	04/19/99	JENNINGS	A TN137

WM01/0710

STEVEN B SAMUELS ESQ
UNISYS CORPORATION
TOWNSHIP LINE & UNION MEETING ROADS
BLUE BELL PA 19424

EXAMINER	
KENDALL, C	
ART UNIT	PAPER NUMBER
2122	

DATE MAILED:
07/10/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/294,617	JENNINGS ET AL.	
	Examiner	Art Unit	
	Chuck O Kendall	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04/19/99*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 April 1999* is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
18) ☐ Interview Summary (PTO-413) Paper No(s). _____.
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

1. This action is in response to the application filed 04/19/99

Claims 1-31 have been examined and rejected.

Information Disclosure Statement

2. The IDS submitted July 21, 1999 has been considered.

Drawings

The drawings filed April 19,1999 were approved as indicated by the Drafts Person, on PTO948.

Common Knowledge

Kernel: The core of an operating system the portion of the system that manages memory, files, and peripheral devices; maintains the time and date; launches applications and allocates system resources. [Microsoft Press Dictionary 3rd edition copy right 1997].

Device driver: A software component that permits a computer system to communicate with a device. In most cases the, the driver also manipulates the hardware in order to transmit the data to the device. [Microsoft Press Dictionary 3rd edition copy right 1997].

Specification Objection

The disclosure is objected to because of minor informalities. It is unclear as to what is inferred to as E-mode (page6,line 19). Examiner has interpreted it as Emulation mode. Appropriate correction or clarification is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (c) he has abandoned the invention.
>
> (d) the invention was first patented or caused to be patented, or was the subject of an inventor's certificate, by the applicant or his legal representatives or assigns in a foreign country prior to the date of the application for patent in this country on an application for patent or inventor's certificate filed more than twelve months before the filing of the application in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claim(1,9,19) rejected under 35 U.S.C. 102(e) as being anticipated by **Dunn** et al [USPN 6,247,172 B1] referenced as **Dunn.**

Claim 1

Dunn anticipates a method for emulating the execution of a target program comprising instructions of an instruction set of a target computer on a host computer having a different instruction set, said method comprising: *(abstract)*

performing a static translation of the instructions of the target program into a series of instructions of an intermediate instruction set, the intermediate instruction set being optimized for interpretation on the host computer; and [*(abstract) also col.1 line 13-15].*

executing the series of instructions of the intermediate instruction set by interpretation on the host computer. (*abstract*).

Claim 9

An emulation system for emulating the execution of a target program comprising instructions of an instruction set of a target computer on a host computer having a different instruction set, said emulator comprising: *(abstract)*

a code translator that performs a static translation of the instructions of the target program into a series of instructions of an intermediate instruction set, the intermediate instruction set being optimized for interpretation on the host computer; and (abstract *also col.1 line 13-15).*

an interpreter that executes the series of instructions of the intermediate instruction set by interpretation on the host computer. *(abstract)*

Claim 19

A computer-readable medium having stored thereon program code that when executed by a host computer enables the host computer to emulate the execution of a target program comprising instructions of an instruction set of a target computer on the host computer, wherein the host computer has a different instruction set, by: abstract

performing a static translation of the instructions of the target program into a series of instructions of an intermediate instruction set, the intermediate instruction set being optimized for interpretation on the host computer; and abstract *also col.1 line 13-15.*

executing the series of instructions of the intermediate instruction set by interpretation on the host computer. abstract

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims (2-8,10-18,20-31) are rejected under 35 U.S.C. 103(a) as being unpatentable over **Dunn** et al [USPN 6,247172 B1] referenced as Dunn in view of **James R. Gillig,** "Endian-Neutral Software, Part 2", published November 1,1994,referenced as **Gillig.**

Claim 2

Dunn discloses a method per claim 1. **Dunn** does not explicitly disclose mapping control words of the instruction set of the target machine into the fundamental word size of the host machine. However, **Gillig** does disclose using an Endian Neutral engine for mapping control words of the instruction set of target machine to the Host machine. Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to combine the teachings of **Dunn** and **Gillig** because, being able to convert from one instruction format to another provides portability (**Gillig**, 1st page, 1st paragraph).

Claim 3

The method recited in claim 1, wherein the intermediate instruction set comprises a plurality of control words that are derived by redefining control words of the target computer to minimize the number of masking and shifting operations needed to decode the plurality of control words of the intermediate instruction set. [***Gillig***, part 2, page 1.2nd paragraph]

Claim 4

The method recited in claim 1, wherein the intermediate instruction set comprises a plurality of different types of control words having formats defined to minimize the time needed to determine the type of a control word. [***Gillig***, part 2, page 6.1st - 3rd paragraph].

Claim 5

The method recited in claim 1, wherein the intermediate instruction set comprises a plurality of controls words derived from control words of the instruction set of the target machine in a manner that reduces the number of different forms of control words in the intermediate instruction set.[***Gillig,*** part 2, page 6].

Claim 6

The method recited in claim 1, wherein a code structure of the intermediate instruction set comprises code words have a fixed length that matches the fundamental word size of the host machine.[***Gillig***,_part 2, page 2 4th paragraph].

Claim 7

The method recited in claim 1, wherein the instructions of the intermediate instruction set have a fixed length and do not cross code word boundaries. [***Gillig,*** part 2,4th paragraph, page 2].

Claim 8

The method recited in claim 1, wherein zero-address instructions of the instruction set of the target machine for pushing data onto a stack for use in a subsequent zero-address instruction operation are incorporated as explicit addresses into a new instruction in the intermediate instruction set for performing that operation, thereby reducing the number of different instructions in the intermediate instruction set. *[* ***Gillig*** ,part 1, 2nd paragraph, page 5].

Claim 10

Dunn discloses a method per claim 9. **Dunn** does not explicitly disclose mapping control words of the instruction set of the target machine into the fundamental word size of the host machine. However, **Gillig** does disclose using an Endian Neutral engine for mapping control words of the instruction set of target machine to the Host machine. Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to combine the teachings of **Dunn** and **Gillig** because, being able to convert from one instruction format to another provides portability (***Gillig***, 1st page, 1st paragraph).

Claim 11

The emulation system recited in claim 9, wherein the intermediate instruction set comprises a plurality of control words that are derived by redefining control words of the target computer to minimize the number of masking and shifting operations needed to decode the

plurality of control words of the intermediate instruction set. [***Gillig*** , part 2, page 1.2nd paragraph].

Claim 12

The emulation system recited in claim 9, wherein the intermediate instruction set comprises a plurality of different types of control words having formats defined to minimize the time needed to determine the type of a control word. [***Gillig*** , part 2, page 6.1st - 3rd paragraph].

Claim 13

The emulation system recited in claim 9, wherein the intermediate instruction set comprises a plurality of controls words derived from control words of the instruction set of the target machine in a manner that reduces the number of different forms of control words in the intermediate instruction set [***Gillig***, part 2, page 6].

Claim 14

The emulation system recited in claim 9, wherein a code structure of the intermediate instruction set comprises code words having a fixed length that matches the fundamental word size of the host machine .[***Gillig***, part 2, page 2 4th paragraph].

Claim 15

The emulation system recited in claim 9, wherein the instructions of the intermediate instruction set have a fixed length and do not cross code word boundaries. *[**Gillig**, part* 2,4th paragraph, page 2].

Claim 16

The emulation system recited in claim 9, wherein the code translator runs as a user mode process under control of a host operating system on the host computer, and wherein the interpreter runs as a kernel mode driver thread under the host operating system. **[*Dunn*,** *abstract].*

Official notice is taken on the use of a kernel mode driver thread in an operating system, which is old and well known in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a kernel mode driver thread in a host operating system, since the kernel is the portion of the system that manages and maintains memory and systems resources.

Claim 17

The emulation system recited in claim 9, wherein the emulation system may comprise multiple instances of the interpreter each running as a different thread in the kernel space of the host operating system. [***Gillig*** part 2, page 6.1st - 3rd paragraph].

Official notice is taken on the use of a kernel mode driver thread in an operating system, which is old and well known in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a kernel mode driver thread in a host operating system, since the kernel is the portion of the system that manages and maintains memory and systems resources.

Claim 18

The emulation system recited in claim 9, wherein zero-address instructions of the instruction set of the target machine for pushing data onto a stack for use in a subsequent zero address instruction operation are incorporated as explicit addresses into a new instruction in the intermediate instruction set for performing that operation, thereby reducing the number of different instructions in the intermediate instruction set. *[**Gillig**,* part 1, 2nd paragraph, page 5].

Claim 20.

Dunn discloses a method per claim 9. **Dunn** does not explicitly disclose mapping control words of the instruction set of the target machine into the fundamental word size of the host machine. However, **Gillig** does disclose using an Endian Neutral engine for mapping control words of the instruction set of target machine to the Host machine. Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to combine the teachings of **Dunn** and **Gillig** because, being able to convert from one instruction format to another provides portability (***Gillig***, 1st page, 1st paragraph).

Claim 21

The computer-readable medium recited in claim 19, wherein the intermediate instruction set comprises a plurality of control words that are derived by redefining control words of the target computer to minimize the number of masking and shifting operations needed to decode the plurality of control words of the intermediate instruction set. [***Gillig*** part 2, page 1.2nd paragraph].

Claim 22

The computer-readable medium recited in claim 19, wherein the intermediate instruction set comprises a plurality of different types of control words having formats defined to minimize the time needed to determine the type of a control word [***Gillig*** part 2, page 6.1st - 3rd paragraph].

Claim 23

The computer-readable medium recited in claim 19, wherein the intermediate instruction set comprises a plurality of controls words derived from control words of the instruction set of the target machine in a manner that reduces the number of different forms of control words in the intermediate instruction set. [***Gillig***, part 2, page 6].

Claim 24

The computer-readable medium recited in claim 19, wherein a code structure of the intermediate instruction set comprises code words have a fixed length that matches the fundamental word size of the host machine [***Gillig***, part 2, page 2 4th paragraph].

Claim 25

The computer-readable medium recited in claim 19, wherein the instructions of the intermediate instruction set have a fixed length and do not cross code word boundaries. *[Gillig* part 2,4th paragraph, page 2].

Claim 26

The computer-readable medium recited in claim 19, wherein zero-address instructions of the instruction set of the target machine for pushing data onto a stack for use in a subsequent zero-address instruction operation are incorporated as explicit addresses into a new instruction in the intermediate instruction set for performing that operation, thereby reducing the number of different instructions in the intermediate instruction set.[*Gillig*, part 1, 2nd paragraph, page 5].

Claim 27.

Dunn discloses a method for defining an intermediate instruction set based on the instruction set of a target machine for use in an emulation system in which a target program, which comprises instructions of the target machine instruction set, is executed by emulation on a host computer having a different instruction set by (i) performing a static translation of the instructions of the target program into a series of instructions of the intermediate instruction set, and then (ii) executing the series of instructions of the intermediate instruction set by interpretation on the host computer, wherein the intermediate instruction set is optimized for interpretation on the host computer and redefining control words of the instruction set of the target machine to reduce the number of different forms of control words in the intermediate instruction set; and defining a code structure of the intermediate instruction set in which code words of that structure have a fixed length that matches the fundamental word size of the host machine.

Dunn does not explicitly disclose mapping control words of the instruction set of the target machine into the fundamental word size of the host machine. However, **Gillig** does disclose using an Endian Neutral engine for mapping control words of the instruction set of target machine to the Host machine. Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to combine the teachings of **Dunn** and **Gillig** because, being able to convert from one instruction format to another provides portability (***Gillig***, 1st page, 1st paragraph).

Claim 28

The method recited in claim 27 wherein said step of mapping control words further comprises redefining control words of the instruction set of the target computer in the

intermediate instruction set to minimize the number of masking and shifting operations needed to decode the control words of the intermediate instruction set. [***Gillig*** part 2, page 1 ,2nd paragraph].

Claim 29

The method recited in claim 27 wherein said step of mapping control words further comprises redefining control words of the instruction set of the target computer in the intermediate instruction set to minimize the time needed to determine the type of a control word of the intermediate instruction set. [***Gillig*** part 2, page 6.1st - 3rd paragraph].

Claim 30

The method recited in claim 27, further comprising defining a set of instructions of the intermediate instruction wherein the instructions have a same fixed length and do not cross code word boundaries. [***Gillig***, part 2,4th paragraph, page 2].

Claim 31

The method recited in claim 27, further comprising incorporating zero-address instructions of the target machine instruction set for pushing data onto a stack for use in a subsequent zero-address instruction operation, as explicit addresses in a new instruction in the intermediate instruction set for performing that operation, thereby reducing the number of different instructions in the intermediate [***Gillig***, part 1, 2nd paragraph, page 5].

Conclusion

The prior art made of record and not relied upon is pertinent to applicant's disclosure.

Correspondence Information

Any response to this action should be mailed to: **Office of the Commissioner of Patents and Trademarks Washington, D.C. 20231**

Any response to this action may be sent via facsimile to either: **(703) 308-1396** (for formal communications marked **EXPEDITED PROCEDURE**), or **(703) 308-1396** (for formal communications marked **PROPOSED or DRAFT).**

Hand delivered responses may be brought to:

Sixth floor Receptionist Crystal Park 2

2121 Crystal Drive

Arlington, Virginia 22202

Any inquires concerning this communication or earlier communications from the examiner should be directed to **Chuck O. Kendall** who may be reached via telephone at (703) 308-6608. The examiner can normally be reached Monday through Friday between 8:30 A.M. and 5:00 P.M. est.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Mark R. Powell**, may be reached at **(703) 305-9703.** Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group. receptionist whose telephone number is **(703) 305-3900.**

Chuck O. Kendall

Mark R. Powell

MARK R. POWELL
SUPERVISORY PATENT EXAMINER
GROUP 2700